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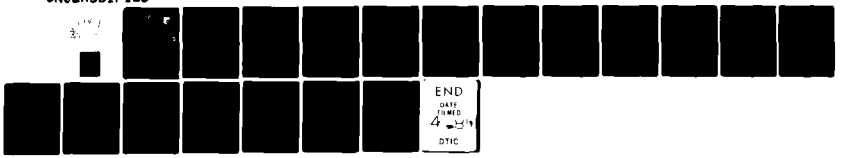

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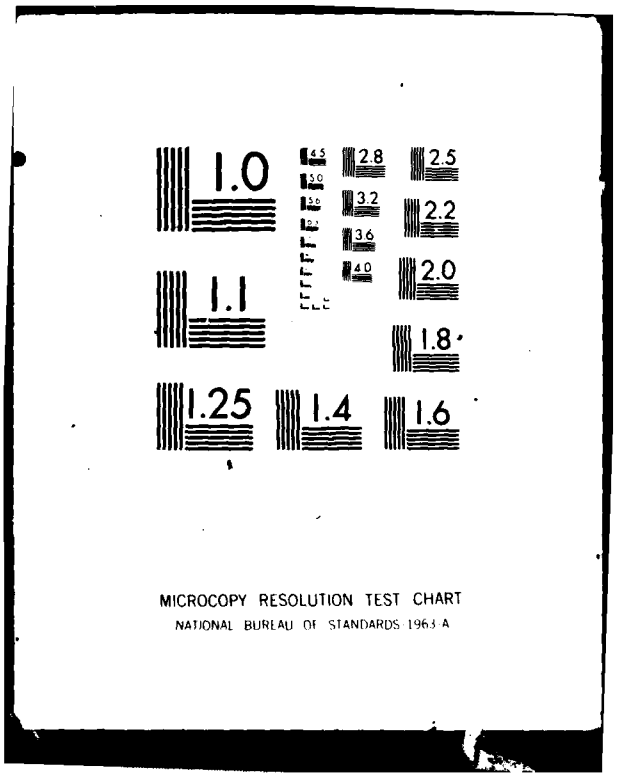
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LEVEL II

GaAs SURFACE PASSIVATION FOR DEVICE APPLICATIONS

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October 1980

Technical Report AFWAL-TR-80-1149
Interim Report for period 15 June 1979 through 14 December 1979

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This report describes the progress in the second six-month period of a program to develop deposited dielectrics for GaAs device applications. Three applications of the dielectrics are being investigated: (1) isolation of control electrodes, (2) passivation of the GaAs surface, and (3) encapsulation of completed circuits. The dielectrics being studied include silicon oxynitride; mixtures of silicon nitride and garmanium nitride; and mixtures of silicon dioxide, gallium oxide, and aluminum oxide.

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and germanium nitride; and mixtures of silicon dioxide, gallium oxide, and aluminum oxide. During this reporting period, studies of the interface properties of pyrolytically deposited Si_3N_4 on n-type GaAs under illuminated conditions were performed. The data obtained are consistent with the interpretation that inversion of the GaAs surface is being achieved. In addition, process parameters for plasma-enhanced deposition of silicon nitride films with low oxygen content and refractive index near that of stoichiometric Si_3N_4 were determined. Evaluation of the interface properties of SiO_2 films deposited on GaAs by photochemical deposition is also reported.

PREFACE

The work reported here is supported by the Avionics Laboratory, Wright-Patterson Air Force Base, Ohio, under contract F33615-78-C-1444, Project Number 2305, Task 2305R1. The monitoring engineer is Capt. R.L. Johnson (AFWAL/AADR). The program objective is to investigate the passivation of gallium arsenide and the application of dielectric thin-film overlayers in metal-insulator-semiconductor field-effect transistors.

This work is being performed jointly by Hughes Research Laboratories, Malibu, CA 90265 and the Technology Support Division of the Hughes Aircraft Company, Culver City, CA 80230. Contributions to this work have been made by C.L. Anderson, M.D. Clark, J.W. Peters, R.A. Jullens, and F.L. Gebhart.

This is the third interim report. The first and second were published as AFAL-TR-79-1057 and AFAL-TR-79-1234, respectively, with the same title. This report covers the period from 15 June 1979 through 14 December 1979. The submittal date of this report was July 1980.

TABLE OF CONTENTS

SECTION 1

INTRODUCTION AND SUMMARY

The goal of this program is to develop dielectrics that will serve the following three basic purposes in gallium arsenide device technology:

- Passivation — reduction of the number of electrically active centers ("surface states") at the semiconductor surface so that the surface potential can be modulated by control electrodes ("gates") overlying the dielectric.
- Isolation — insulation of control electrodes from each other and from the substrate.
- Encapsulation — overcoating of operational circuits to reduce their sensitivity to environmental influences.

To serve these three purposes, Hughes Aircraft Company is developing a variety of deposited dielectrics. Techniques for depositing these dielectric materials are being developed under Hughes internal funding. Evaluation and optimization of these materials for GaAs device applications are being performed under the subject contract.

The following materials are being developed:

- $Ga_xAl_yO_z$ (gallium-aluminum oxide), referred to as (Ga,Al)O
- $Ga_xSi_yO_z$ (gallium-silicon oxide), or (Ga,Si)O
- $Al_xSi_yO_z$ (gallium-silicon oxide), or (Ga,Si)O
- $Al_xSi_yO_z$ (aluminum-silicon oxide), or (Al,Si)O
- SiO_xN_y (silicon oxynitride)
- (Si, Ge)N (silicon-germanium nitride).

Three basic techniques for depositing these materials are being evaluated:

- Pyrolytic chemical vapor deposition (CVD)
- Plasma-enhanced deposition (PED)
- Photochemical deposition (PCD).

We reported in AFAL-TR-79-1057 the successful use of our proprietary plasma-deposited glass as an isolation dielectric in GaAs MESFET ICs. In AFAL-TR-79-1234, we reported the application of this dielectric as an encapsulant for discrete GaAs MESFETs with the loss of only 0.5 dB gain at 9.7 GHz. Because of the demonstrated utility of this dielectric for isolation and encapsulation applications, this program has been redirected to investigate the application of deposited dielectrics solely for passivation applications.

The results presented in AFAL-TR-79-1057 and in AFAL-TR-79-1234 clearly indicated that the vacuum technology employed in our commercial plasma reactor (LFE Corp. model PND-301) was inadequate for the fabrication of PED "Si_3N_4" and "Ge_3N_4" with acceptably low oxygen content for passivation applications. The MIS C-V characteristics presented in AFAL-TR-79-1234 strongly suggest that high oxygen content in the deposited films is correlated with poor interface properties, especially "pseudo-inversion." (Pseudo-inversion is the saturation of the capacitance of MIS diodes at values in excess of the theoretical high-frequency inversion capacitance.)

Accordingly, we have designed a PED system whose improved vacuum technology and fixturing should result in the deposition of films with excellent thickness uniformity and composition control. This system, which can simultaneously deposit films on four 5-cm-diameter wafers, was described in AFAL-TR-79-1234. During this report period, we have employed one technician nearly full time in constructing this system under Hughes internal funding. By the end of the period, mechanical assembly of the system was complete. Application of this system to film depositions for this program will begin in the next reporting period.

Pending completion of the new PED system, PED studies on this program were suspended during this reporting period. Accordingly, we concentrated our studies in two areas: development of etching procedures that result in minimal interfacial oxide layers and evaluation of pyrolytic Si_3N_4 as an MIS passivation dielectric.

Our etching studies were based on ellipsometric analysis of several etches performed after a standard cleaning procedure. These

studies indicated that anodic oxide growth followed by removal of the oxide in 1M NH_4OH yields the optimum combination of low residual oxide thickness and surface morphology. These studies are described in Section 2.

During this report period, a process for depositing pyrolytic Si_3N_4 at 615°C was established and films of this material were evaluated for passivation applications using MIS C-V analysis. The C-V data exhibit moderate frequency dispersion in the accumulative regime, some pseudo-inversion, and the ability to achieve stable deep depletion. These results are reported in Section 3.

During this report period, we continued to upgrade the diagnostic equipment committed to this program. A Hewlett-Packard model 4275A multifrequency LCR meter was integrated into our digital C-V/G-V system. The present capabilities of the system are described in Section 4.

SECTION 2

CLEANING AND ETCHING PROCEDURES

The application of deposited dielectric films to the passivation of GaAs for device applications relies on the premise that the surface "oxide" film of unknown composition that exists on the sample surface immediately prior to the deposition of the dielectric is sufficiently thin and tenuous that the surface properties can be controlled by the deposited dielectric. Accordingly, the development of surface cleaning and etching procedures which result in a thin "oxide" layer of reproducible properties was addressed during this report period.

Prior to the final surface etching step, all samples were cleaned by a standard cleaning procedure designed to remove organic contaminnants and any excess Ga on the wafer surface resulting from epitaxial growth. This cleaning procedure, which has been found to be successful for a wide variety of applications, is described in Table 1.

To investigate the effectiveness of etching for minimizing residual oxide, we utilize our Gaertner L116 ellipsometer to measure the apparent complex index of refraction, $N_s^* = N_s + iK_s$, of the substrate immediately after etching. Neither the thickness nor the index N_f of a very thin film can be precisely determined unless a true N_s^* is accurately known. Unfortunately, N_s^* is not known with sufficient accuracy to permit such a detailed analysis. However, the effect of a thin, transparent film on the measured N_s^* is to decrease N_s and increase $|K_s|$ over that of an ideal substrate ($K_s < 0$ for an absorbing substrate). This will be the case for $1 < N_f < N_s$, assuming $|K_s| \ll N_s$. From our measurements, together with published absorption data, our best estimate of the ideal N_s^* of GaAs at a 632.8 nm wavelength is 3.89 - 0.19i. For an oxide film, we expect $N_f < 3.89$ so that the effectiveness of an etch can be judged by the degree to which it minimizes $|K_s|$ and maximizes N_s. The value of K_s is the most sensitive indicator of a surface film.

Table 1. Cleaning Procedure for GaAs Wafers

Distinguish four categories and modify general cleaning procedure per instructions below.

A. New polished wafers

B. Epitaxial wafers

C. Ion implanted wafer not yet annealed

D. Photoresist processed wafers

General Procedure:

1. Tricholoroethylene (TCE) to boiling (boil 3 min)
2. TCE to boiling (boil 3 min)
3. Cold methanol/acetone dip (80% acetone/20% methanol)
4. DI H_2O rinse (1 min)
5. 50% HCl/DI H_2O (3 min)
6. DI H_2O rinse (2 min)
7. Isopropyl to boiling (boil 2 min)
8. Blow or spin dry
9. Inspect

Category A: Complete procedure

Category B: Change step 5 only if excess Ga is present. Use hot 50% HCl/DI H_2O, but do not boil.

Category C: Eliminate steps 4 and 5.

Category D: Change step 3 to boiling acetone (3 min).

Note: Use only the following solvents and chemicals: Allied Chemicals, Semiconductor Low Mobile Ion Grade Mallinckrodt, Transistor Grade

DI H_2O — 18 mΩ

Or as approved by supervisor.

The initial etches evaluated were NH_4OH:30% H_2O_2:H_2O (5:2:240 by volume) and 1 M NaOH:0.76 M H_2O_2 (1:1 by volume). The substrates were undoped n-type bulk-grown GaAs. After cleaning by the procedure given in Table 1, samples were etched for 2 min at room temperature, rinsed in DI H_2O, and dried in flowing N_2 gas. Ellipsometric measurements were made immediately thereafter. N_s^* was measured for an array of points on each sample. Measurements were completed within a few minutes after etching.

From these data, average values and standard deviations were computed. The results, shown in Table 2, indicate that the NH_4OH:H_2O_2 etch leaves the least oxide, whereas the NaOH:H_2O_2 etch is slightly more uniform.

During our cleaning studies, we encountered several wafers of GaAs that were heavily contaminated with particulate matter and "scum" that had apparently resulted from the use of improper packing material by the suppliers. The solvent/HCl cleaning procedure of Table 1 was not completely effective for removing these heavy deposits since such deposits are not normally encountered on polished GaAs wafers.

Table 2. Surface Optical Properties After Etching Without Anodization or Stripping

Etch	Number of Measurements	$\bar{N}_s$	$\sigma(N_s)$	$\bar{K}_s$	$\sigma(K_s)$
NH_4OH:H_2O_2:H_2O					
Sample No. 1	26	3.876	0.011	-0.280	0.051
Sample No. 2	16	3.861	0.007	-0.336	0.035
NaOH:H_2O_2					
Sample No. 1	23	3.829	0.008	-0.322	0.024
Sample No. 2	12	3.820	0	-0.375	0.016

We found that most of the remaining contamination could be effectively removed by growing about 100 nm of native anodic oxide and then etching away the oxide with 1M NH_4OH. The oxide is grown at room temperature in an electrolyte of composition 17 g ammonium pentaborate per 100 ml of ethylene glycol. A proprietary method is used to electrically contact the back side of the wafer so that the entire front side can be anodized. To ensure uniformity, the wafer is illuminated during anodization. The cathode of the anodization cell is Pt foil.

Several etchants were evaluated on wafers that had received this additional anodization/stripping step after the Table 1 cleaning procedure. Effectiveness was judged by ellipsometry as described above. The following etches were evaluated:

(1)	NH_4OH: 30% H_2O_2:H_2O	(5:2:240)
(2)	1 M NaOH: 0.76 M H_2O_2	(1:1)
(3)	HCl:H_2O: 30% H_2O_2	(1:1 "a few drops")
(4)	BR_2:CH_3OH	(1% Br_2 by volume)
(5)	HF:H_2O	(10% HF by volume)
(6)	HCl:H_2O	(50% HCl by volume)

Etches (5) and (6) attack native oxide but do not etch GaAs at room temperature. These etches generally give comparable results, although Br_2:CH_3OH is somewhat less effective than the others. However, when applied either to samples that have or have not been cleaned by anodic oxide growth and stripping, none of the etches give a surface significantly superior to that obtained by anodic cleaning only. Furthermore, etches (1) through (4), which attack GaAs, cause some degradation of surface morphology because of nonuniform etching, whereas anodic cleaning essentially replicates the original polished surface. Consequently, anodic oxide growth and stripping without subsequent GaAs etching appears to be the best cleaning procedure of those investigated.

SECTION 3

EVALUATION OF PYROLYTIC SILICON NITRIDE FOR GaAs PASSIVATION APPLICATIONS

Our pyrolytic CVD reactor had earlier been moved to a new laboratory; during this period, it was again made operational. After the system was checked out, samples of GaAs coated with pyrolytic CVD Si_3N_4 dielectric were fabricated. The silicon nitride depositions were done in a cold-wall, atmospheric-pressure reactor with an rf-heated susceptor. Gas flow data were as follows:

SiH_4:	11 cm^3/min
NH_3:	3.6 liters/min
N_2 carrier gas:	29 liters/min

Deposition temperature was about 615°C, which gave a deposition rate of about 20 nm/min. The deposition sequence followed involved establishing all gas flows with the sample held at 315°C, after which the sample temperature was ramped up to the deposition temperature in approximately 9 sec. This sequence minimized exposure of the uncoated sample to temperatures at which thermal decomposition of GaAs would occur.

Capacitance-voltage and conductance-voltage data for an Si_3N_4 sample are shown in Figures 1 and 2, respectively. Ellipsometric parameters of the film were n = 1.95 and thickness = 47 nm. Capacitor structures were formed by depositing 0.29-mm-diameter, ∿250-nm-thick Al dots. Substrate material was n-type with a nominal donor concentration of 1.7×10^{15} cm^{-3} and a mobility of 4900 cm^2/V-sec. The C(V) and G(V) measurements were made with the measurement system described in Section 4. The computer program controlling the measurement provides for measurement at 100 voltages covering the range between selected minimum and maximum voltages. Following each change of voltage, C and G are measured for all selected frequencies. The C(V) data of Figure 1 show substantial frequency dispersion for accumulation bias. The 10-MHz data evidently do not represent the high-frequency limit. For inversion bias, there are

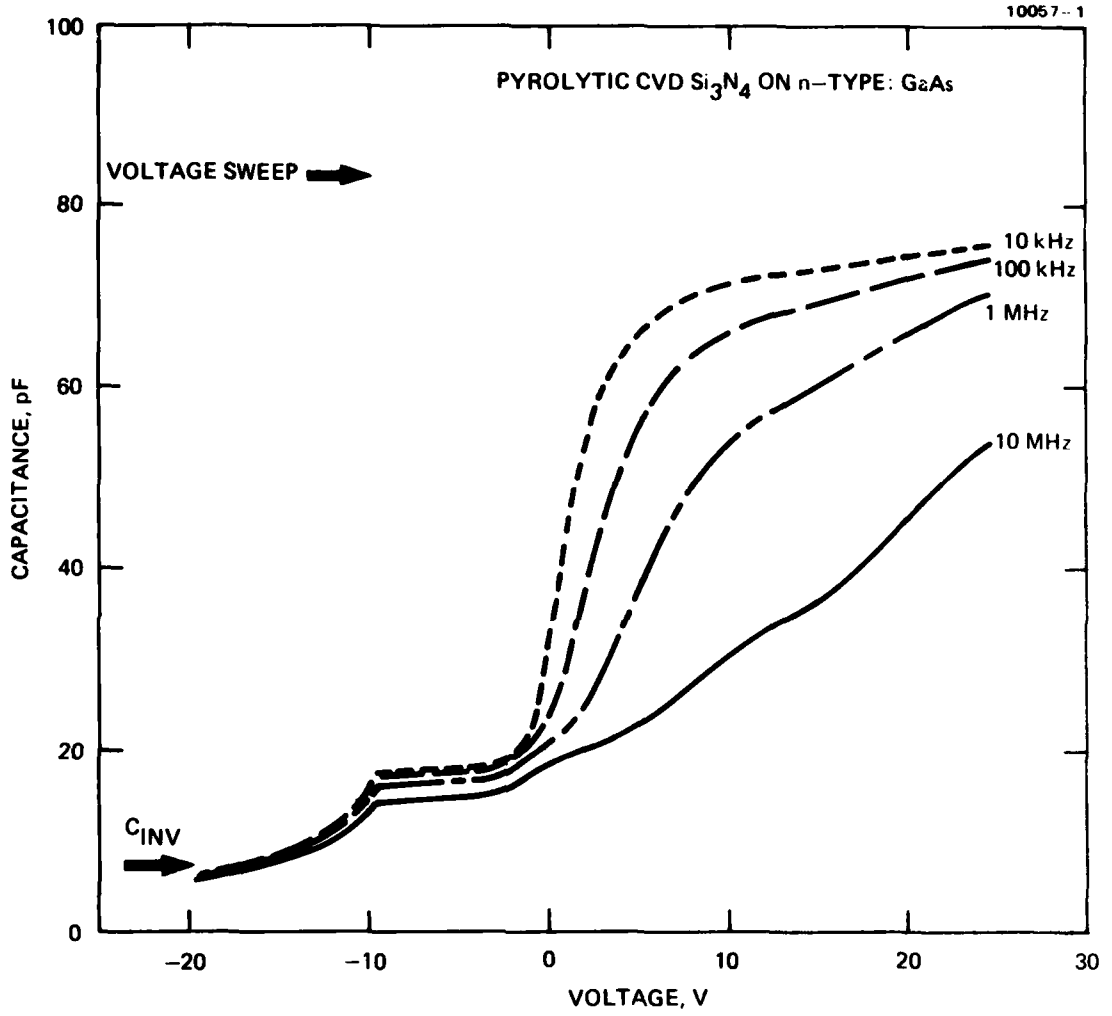

Figure 1. Capacitance of Al-Si_3N_4-GaAs structure as a function of test frequency and Al bias voltage.

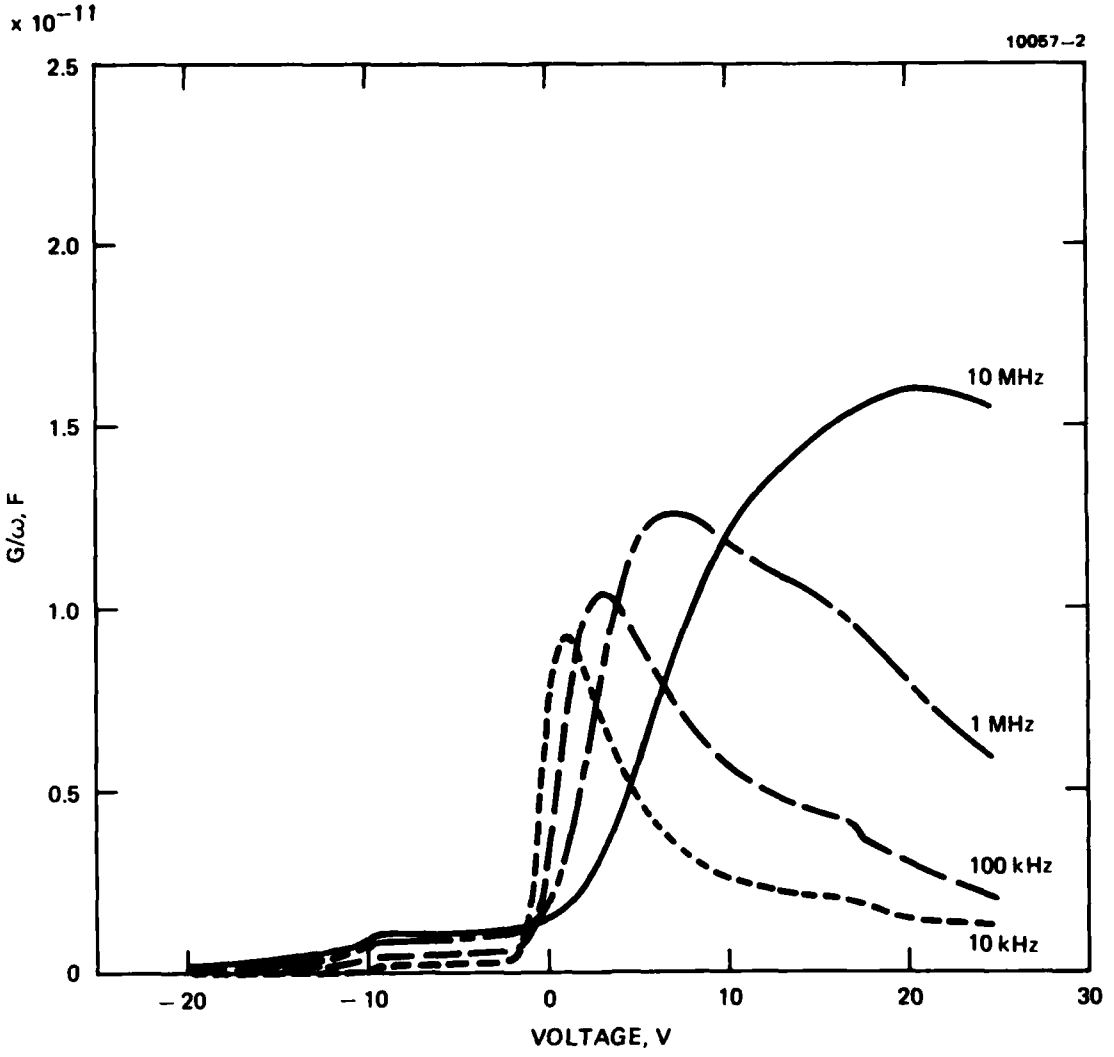

Figure 2. Parallel conductance of Al-Si_3N_4-GaAs structure as a function of test frequency and Al bias voltage.

indications of possible pseudo-inversion behavior between -3 V and -10 V. A theoretical inversion capacitance C_{inv} of 7.3 pF is indicated in Figure 1. This value was computed using the nominal donor concentration of the substrate and an insulator capacitance of 75 pF, which is the largest measured capacitance at 10 kHz. The pseudo-inversion level is substantially greater than C_{inv}. However, beyond -10 V, the capacitance actually drops slightly below C_{inv}, suggesting that a stable deep depletion condition may exist. To avoid a transient deep depletion, the sample was illuminated while biased at -20 V and the illumination was then removed for the voltage scan. We previously have seen indications of stable deep depletion with PED "Si_3N_4" films.

SECTION 4

AUTOMATED CAPACITANCE-VOLTAGE MEASUREMENT SYSTEM

A diagram of the system used for C(V) measurements is presented as Figure 3. All instruments in this system were manufactured by Hewlett-Packard. A model 9825A desktop computer functions as system controller and interfacees to peripheral instruments via an IEEE Standard 488 bus. Device capacitance is measured by a model 4275A multifrequency LCR meter. The test frequency can be set by the controller to any of ten values that span the range from 10 kHz to 10 MHz in a 1-2-4-10 sequence. The test signal level is variable from 1 mV to 1 V rms and is typically adjusted to 20 mV rms for measurement of MIS capacitors at 300°K.

A model 6131C digital voltage source provides the bias voltage that is applied to the sample through internal circuitry of the LCR meter. The bias range is ±99.99 V with four-digit resolution. The model 59301A ASCII-to-parallel converter converts byte-serial data from the bus to the bit-parallel BCD input required by the digial voltage source.

A model 3455A digital voltmeter attached to the "dc bias monitor" jack of the LCR meter measures the bias voltage that appears across the device under test (DUT). This bias measurement is necessary for best accuracy because the LCR circuitry through which the voltage from an external source is applied to the sample includes series resistance. As a result, the bias across the DUT can differ from the programmed voltage of the digial voltage source if significant dc leakage current flows through the DUT.

A shielded probe box was fabricated for probing MIS capacitors. The probe box connects directly to the "Unknown" terminals of the LCR meter so as to minimize lead length for best accuracy at 10 MHz. During measurement, the probes are completely enclosed by the metallic probe box. The sample is thus shielded from both ambient light and electromagnetic interference.

Hard copy data output from the system is obtained as either a graphic plot from the 9872A graphic plotter or numeric printout from the printer of the 9825A desktop computer.

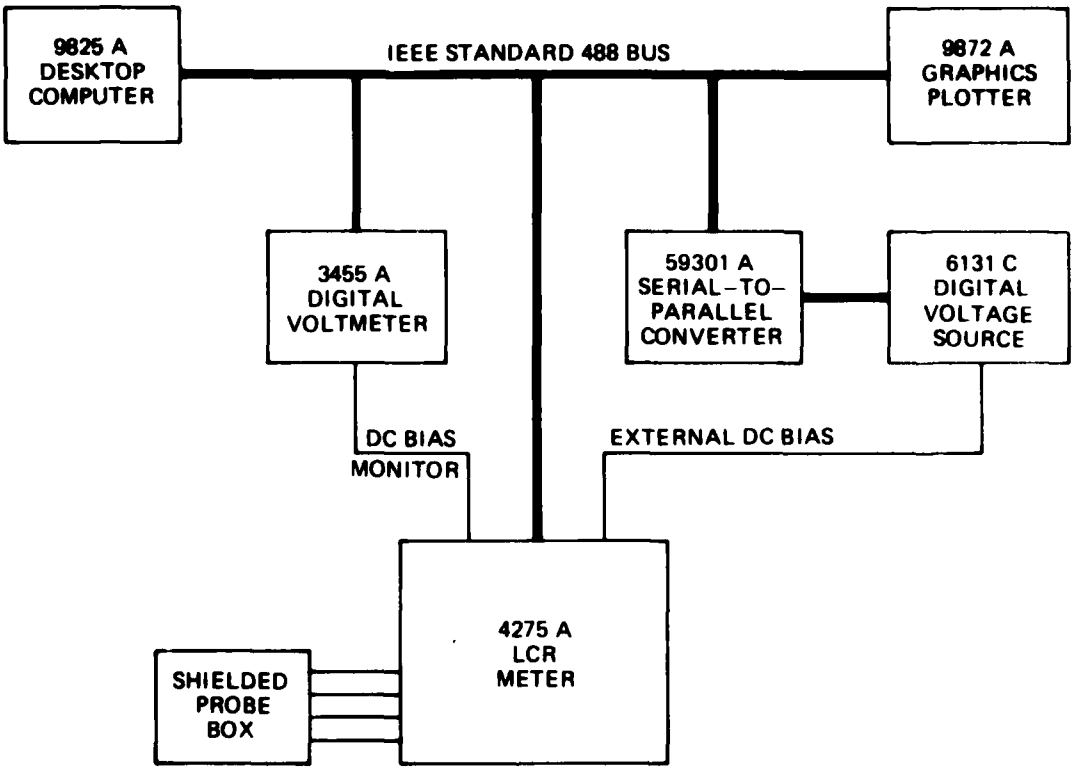

Figure 3. Automated capacitance-voltage measurement system.

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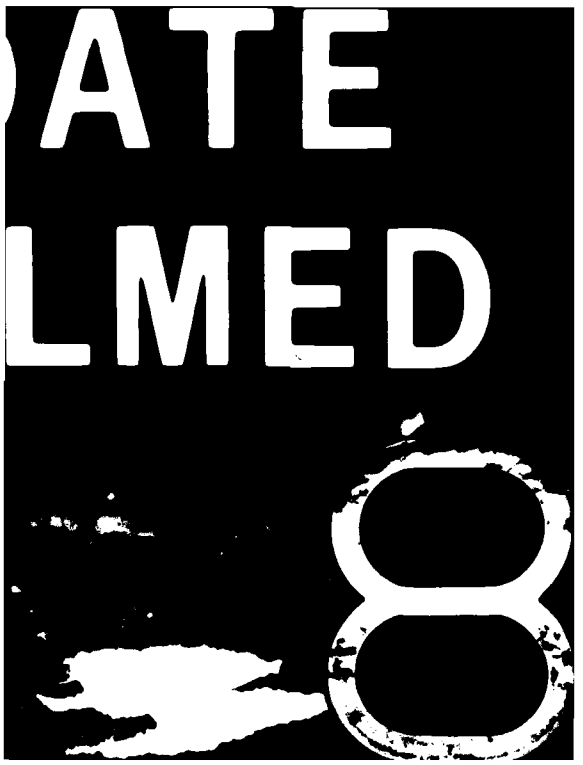
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